TEXAS INSTRUMENTS

SN65HVD22EVM

USER'S GUIDE

March 2003 High-Performance Linear/Interface Products

SLLU057

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the voltage range of 0 V to 5 V for digital input/outputs and within the voltage range of -20 V to +25 V for bus inputs/outputs.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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Chapter 1

Introduction

This user's guide describes the SN65HVD22 Evaluation Module (EVM). The EVM helps designers develop and analyze data transmission systems using the SN65HVD2X family of devices from Texas Instruments. The SN65HVD22 EVM highlights the wide common-mode voltage functionality and robust performance of the SN65HVD22 RS-485 transceiver.

Topic **Page**

1.1 Overview

The transceivers in the HVD2x family offer performance far exceeding typical RS-485 devices. In addition to meeting all requirements of the TIA/EIA-485-A standard, the HVD2x family operates over an extended range common-mode voltage, and has features such as high ESD protection, wide receiver hysteresis, and failsafe operation. This family of devices is ideally suited for long-cable networks and other applications where the environment is too harsh for ordinary transceivers.

These devices are designed for bidirectional data transmission on multipoint twisted-pair cables. Example applications are digital motor controllers, remote sensors and terminals, industrial process control, security stations, and environmental control systems.

These devices combine a 3-state differential driver and a differential receiver, which operate from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a differential bus port that offers minimum loading to the bus. This port features an extended common-mode voltage range making the device suitable for multipoint applications over long cable runs. Figure 1-1 shows the basic functions of the SN65HVD22.

The SN65HVD22 has controlled driver output slew rate for low radiated noise in emission-sensitive applications and for improved signal quality with long stubs. Up to 256 SN65HVD22 nodes can be connected at signaling rates up to 500 kbps.

Figure 1-1. Functional Configurations of the SN65HVD22

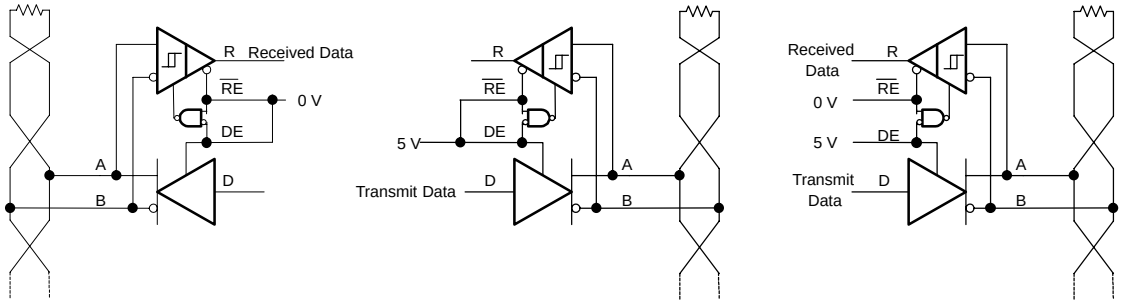
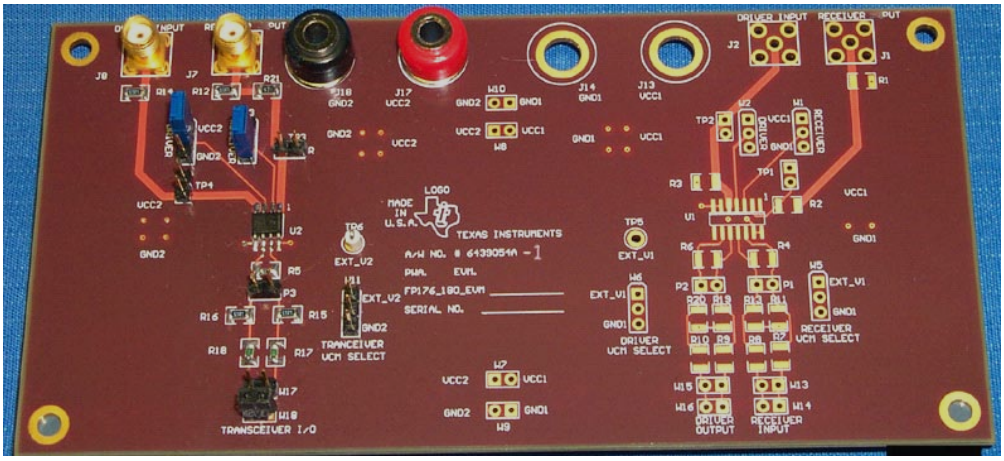


Figure 1-2 is a picture of the SN65HVD22 EVM. The EVM part number is SN65HVD22EVM and comes with the SN65HVD22D (U2) installed. A copy of the data sheet is shipped with the EVM—however, the latest version of the data sheet is available from www.ti.com.

Figure 1-2. SN65HVD22 Evaluation Module (EVM)



Note that the EVM printed circuit board includes a location (U1) for a full-duplex transceiver. This allows for future EVM configurations using the same board.

1.2 Signal Paths

The signal paths on this EVM include coaxial connectors (J7 and J8) for connecting to test equipment, and differential connection points (W17 and W18) for connecting to an RS-485 bus. Two banana jacks (J17 and J18) provide for power and ground connections. Jumpers (W3 and W4) in the circuit can be used to set the transceiver enabling. Jumper W11 is used to select the common-mode voltage (V_{CM}) test conditions. Additional test points are provided in the circuit to facilitate measurements of critical signals.

Table 1-1 lists the EVM connections.

Table 1-1. HVD22 EVM Connections

Connection	Label	Description
J17	Vcc2	Power supply for HVD22 device
J18	GND2	Power supply ground
J7	RECEIVER	Receiver output, R (pin 1)
J8	DRIVER INPUT	Driver input, D (pin 4)
P3, W17, W18	TRANSCEIVER I/O	RS-485 BUS I/O (pins 6 and 7)
TP3	R	Receiver output (pin 1)
TP4		Driver input, D (pin 4)
TP6	EXT_V2	Externally applied Vcm
W3	RECEIVER	Receiver enable, RE, (pin 2)
W4	DRIVER	Driver enable, DE, (pin 3)
W11	TRANSCEIVER VCM SELECT	Select between Vcm choices: None, GND2, External

Chapter 2

EVM Setup and Operation

This chapter describes the setup and operation of the SN65HVD22EVM.

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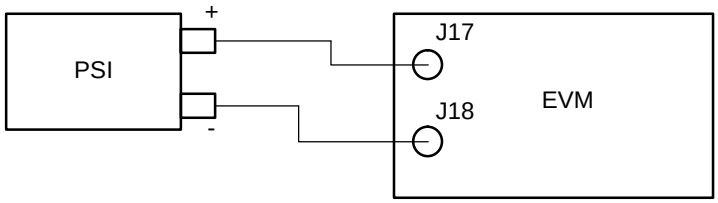
2.1 Single EVM

A single EVM can be used to evaluate the operation and parametric performance of the SN65HVD22 transceiver. The design of the EVM facilitates evaluation using a single 5-V supply. No additional cabling or loads are necessary to evaluate the basic performance of the transceiver. Jumpers are provided to select the mode of operation, discussed below. Ensure the 5-V supply has a current capability of at least 60 mA, and adjust the output to 5 V ± 0.5 V.

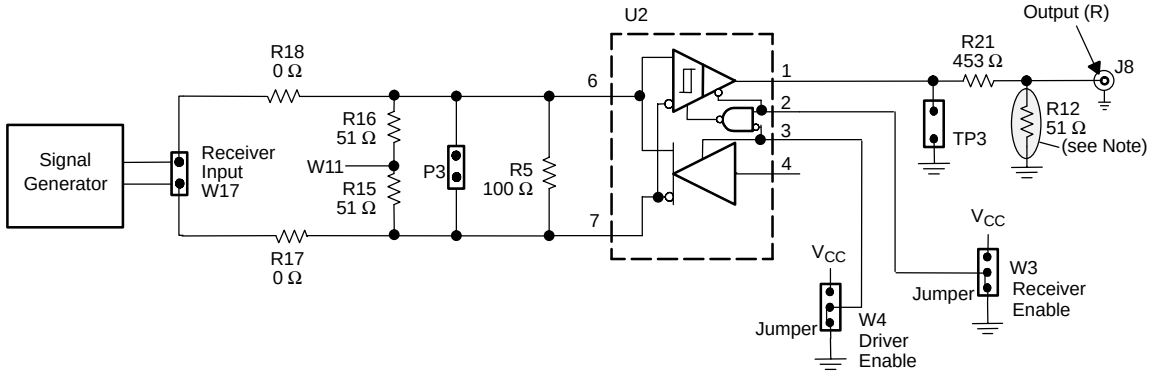
Figure 2-1. EVM Power Connections for Single SN65HVD22 Evaluaton



2.1.1 Receiver Evaluation

The EVM configuration for evaluating the receiver performance is shown in Figure 2-2. Note that jumper W3 is set to enable the receiver, and jumper W4 is set to disable the driver. W11 allows for external application of a common-mode voltage. If W11 is left open, no offset voltage is induced on the test signal.

Figure 2-2. Configuration for Receiver Evaluation



Note: R12 not installed.

The input or output characteristics of the receiver can be observed by probing P3 (receiver input) and TP3 (receiver output). With the driver disabled as shown, the impedance at the signal input W17 is approximately 50 Ω, due to the resistors R5, R15, and R16. This matches the impedance of a standard signal generator with 50-Ω output impedance.

2.1.2 Driver Evaluation

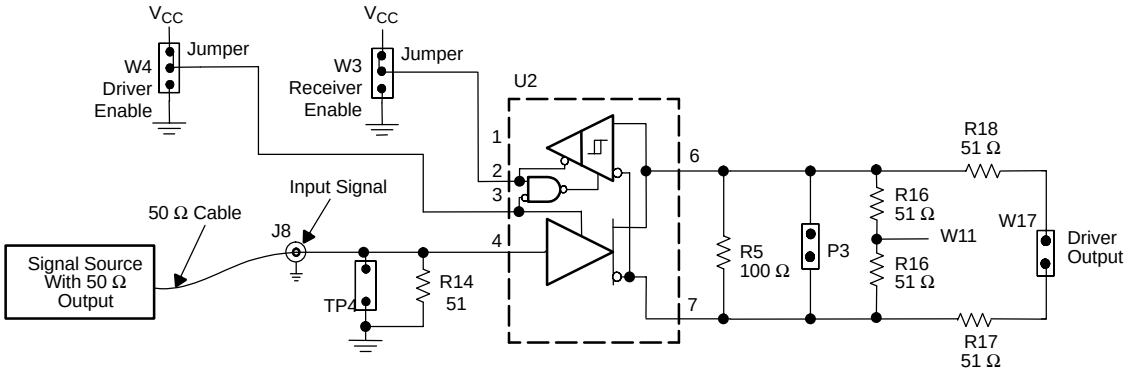
The EVM configuration for evaluating the driver prformance is shown in Figure 2-3. Note that jumper W3 is set to disable the receiver, and jumper W4 is set to enable the driver.

When using a general-purpose signal generator with 50-Ω output impedance, make sure that the signal levels are between 0 V and 5 V with respect to J18, device under test ground (DUT GND), designated as GND2.

Apply the driver input signal (D) to connector J8. Resistor R14 provides termination impedance matched to a standard 50-Ω output- impedance signal generator.

At the driver outputs, the EVM comes with a 100-Ω resistor (R5) installed across the differential outputs, as well as resistors R15 and R16, which add another 102 Ω across the differential outputs. The parallel combination of R5 with R15 and R16 creates a total load of about 50 Ω at the driver outputs.

Figure 2-3. Configuration for Driver Evaluation

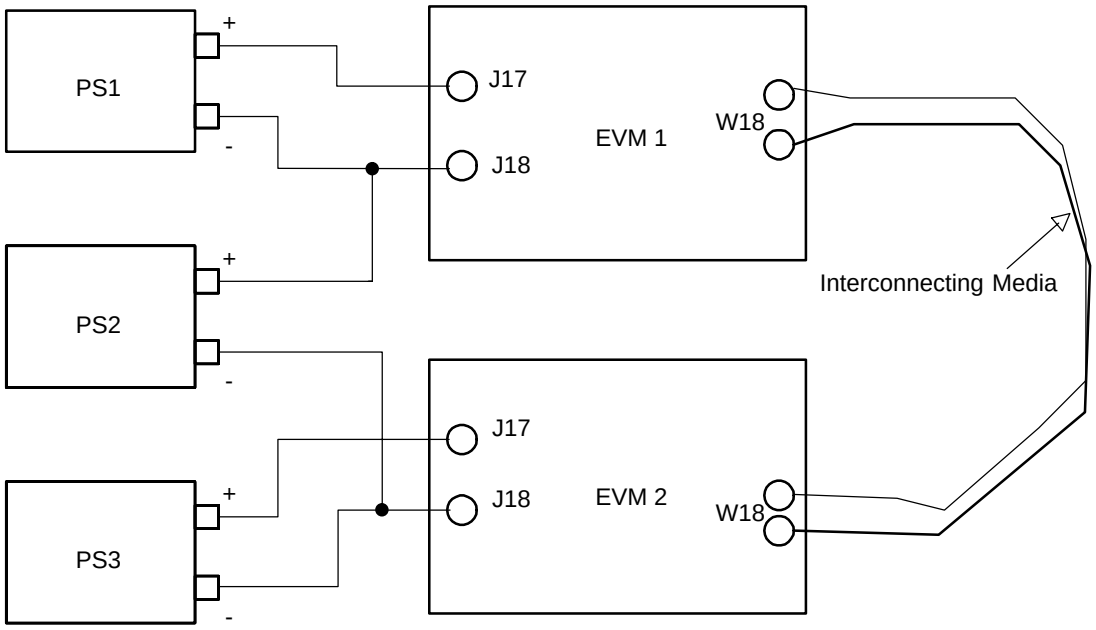


The input/output characteristics of the driver can be observed by probing TP4 (driver input) and either P3 or W17 (driver output). In addition to the single-ended outputs (with respect to GND2) and the differential outputs available at P3 and W17, the common-mode output can be observed using W11 as a test point.

2.2 Demonstration of Operation Over Common-Mode Voltage Range

A unique feature of the HVD2X family is the ability to operate with common-mode voltages in the range from –20 V to 25 V. In order to demonstrate SN65HVD22 operation over the extended range of common-mode voltage, two EVMs are required. Figure 2-4 shows how two EVMs and three power supplies can be used to induce a ground potential difference between EVM1 and EVM2.

Figure 2-4. EVM and Power Supply Setup for Inducing a Ground Potential Difference Between Nodes



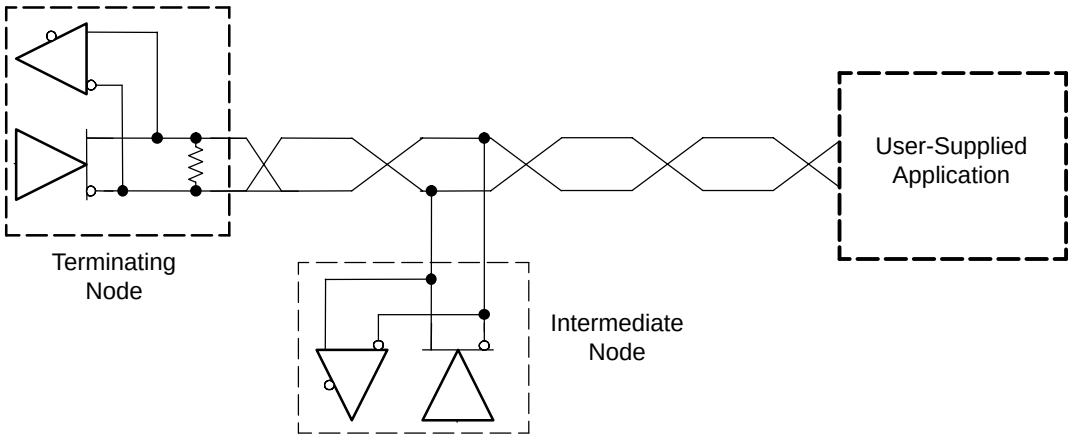
Power supply PS1 supplies the V_{CC2} voltage to EVM1, and power supply PS3 supplies the V_{CC2} voltage to EVM2. Power supply PS2 forces an offset between the ground reference of PS1 and PS3. Special care must be taken to make sure the grounds of the two EVMs are not connected together through instrumentation or non-isolated power supply earth ground or chassis connections. When using more than one probe with this test set up, make only one return connection to the oscilloscope.

When used in this configuration, remove resistor R5 from each EVM to provide single termination at each end of the bus.

2.3 Evaluation With User-Supplied Application

The EVM can also be used to evaluate the performance of the transceiver with an existing or prototype RS-485 system. The EVM can be configured as discussed above, and connected to the bus of interest. Depending on the system configuration, EVM termination resistors may need to be removed to ensure correct termination. If the EVM is used as a terminating node (at one end of the bus), remove only R5. If the EVM is used as an intermediate node (not at either end of the bus), remove R5, R15, and R16, and locate termination resistors at each end of the bus. These options are illustrated in Figure 2-5.

Figure 2-5. EVMs With User-Supplied Application



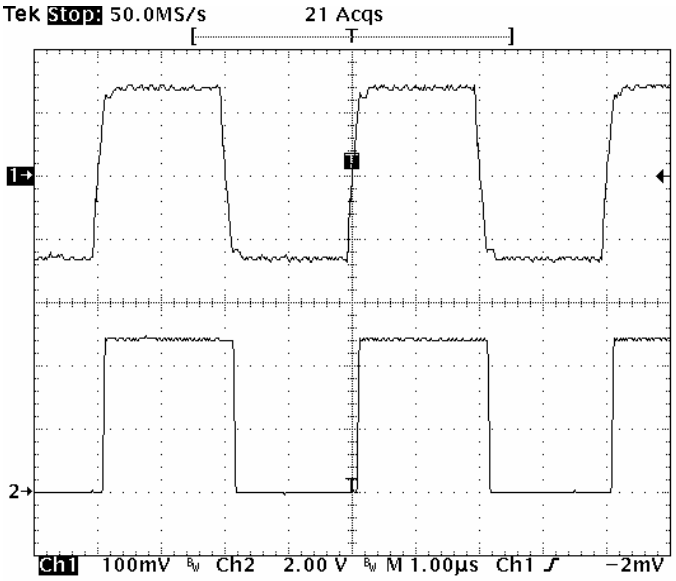
Note that correct termination is assumed in the user-supplied application.

2.4 Typical Test Results

2.4.1 Differential Receiver Operation

A typical result obtained with the EVM configured to operate as a differential receiver is shown in Figure 2-6. The upper waveform (channel 1) is the bus differential voltage across the receiver inputs (A and B). Note the amplitude of the input signal transitions between 140 mV and -140 mV at a signaling rate of 500 kbps (2 μs bit time). The lower waveform (channel 2) is the single-ended output of the receiver (R).

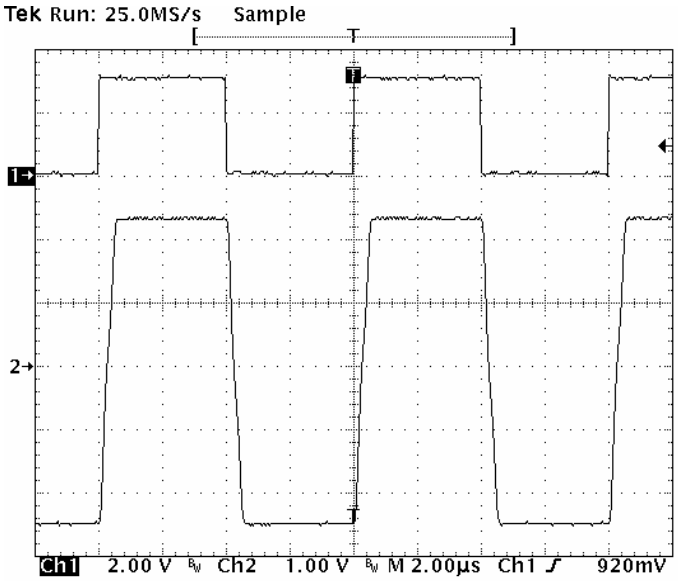
Figure 2-6. Example Waveforms Showing Typical Differential Receiver Operation



2.4.2 Differential Driver Operation

A typical result obtained with the EVM configured to operate as a differential driver is shown in Figure 2-7. The upper waveform (channel 1) is the single-ended input to the driver (D). The lower waveform (channel 2) is the differential voltage of the two driver outputs (V_A-V_B). Note the amplitude of the output signal transitions between 2.3 V and –2.3 V at a signaling rate of 250 kbps (4 μs bit time)

Figure 2-7. Example Waveforms Showing Typical Differential Driver Operation



The effect of the driver slew rate limit is also evident when using the EVM in this configuration. The slope of the driver transitions is controlled to reduce high frequency content, which may create problems in long cable applications. The slew-rate control is designed for signaling rates up to 500 kbps in the SN65HVD22.

2.4.3 Common-Mode Voltage Operation

To demonstrate the performance of these transceivers across various common-mode voltages, setup two EVMs as shown in Figure 2-8. Note that special care is taken to isolate the ground paths, allowing the ground reference of the receiving EVM to be offset relative to the ground of the driving EVM. Figure 2-9 illustrates typical results with two EVMs configured with common-mode voltage as shown in the circuit of Figure 2-8. The upper waveform (channel 1) is the differential signal on the bus lines (A and B) measured at W17. This signal is input to the receiver through a twisted pair. The lower waveform (channel 2) is the output of the receiver. Note that the vertical alignment of the ground reference for both channel 1 and channel two has been set at the same point, so the voltage offset can be read directly.

Figure 2-8. Set-Up for Operation Using Two EVMs With Common-Mode Voltage Difference

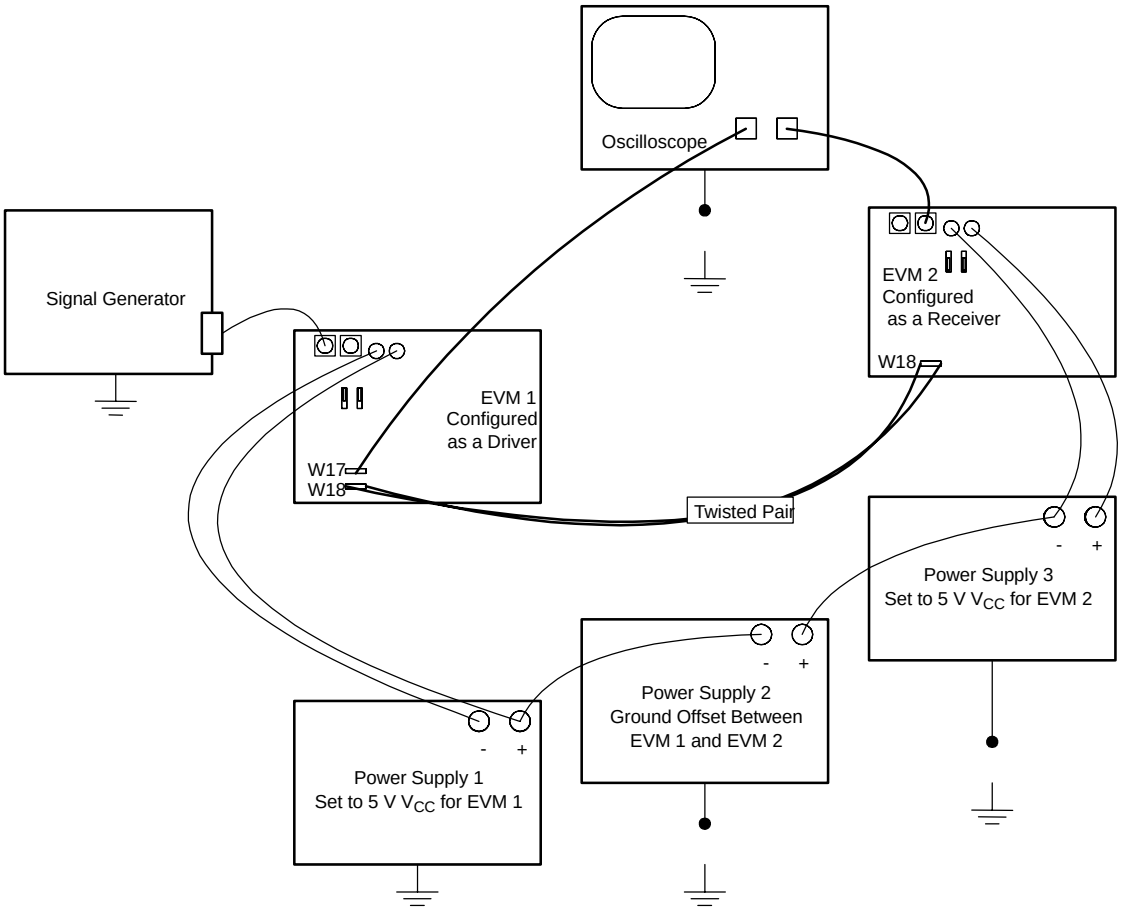
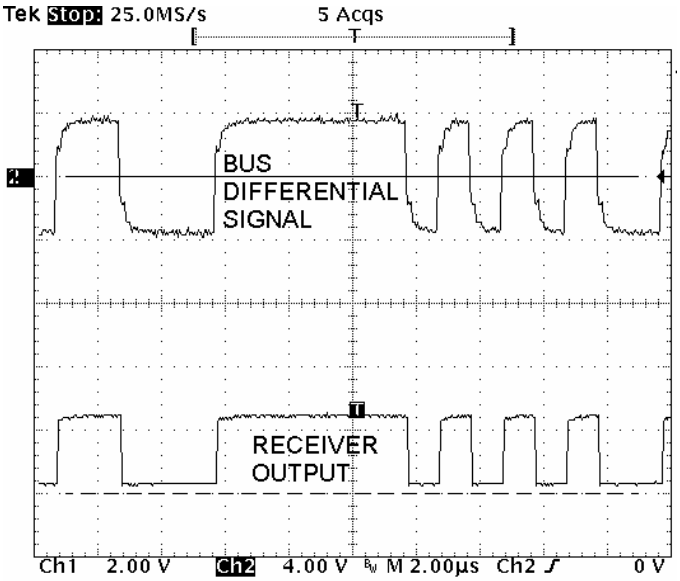


Figure 2-9. Example Waveforms, Showing Typical Extended Common-Mode Voltage Operation



In this example, the oscilloscope cursors are used to indicate the 20-V offset that has been induced between the driver on one EVM and the receiver on another. This demonstrates the performance of the SN65HVD22 with offsets exceeding the capabilities of standard transceivers.

Figure 2-9 also illustrates the capability of using the EVM to evaluate transceiver performance in conjunction with various cable lengths, and/or various cable types. Note the degradation of the signal transitions on channel 1, due to the effects of the lossy transmission line.

Chapter 3

EVM Construction

This chapter describes the SN65HVD22EVM construction and includes the bill of materials and schematic diagram.

Topic **Page**

3.1 Board Layout Patterns

The printed wiring board (PWB) layout for the EVM is designed according to good engineering practices for data transmission circuits. Designers can use this layout as a guide for their applications. Special considerations include:

1) Balanced traces for the differential signals—the connections to the differential bus should be kept balanced, so that the electrical characteristics of one input/output (A or B) are identical to the other. This ensures that all electrical noise is coupled onto both channels nearly equally, allowing the transceiver to perform with optimum noise immunity.

2) Keeping stub length short—the electrical connections between the transceiver and the main bus lines. This reduces reflections from signal transitions. A rule of thumb is to keep the stub electrical length, in terms of propagation delay, less than 40% of the signal transition time. [See also the Texas Instruments Design Note Interface Circuits for TIA/EIA-485 (RS-485)].

3) Ground and power planes may be used to help reduce electrical noise in the system.

Figure 3-1. PWB Fabrication Notes and Stackup

Notes:

1) PWB to be fabricated to met or exceed IPC-6012, Class 3 standards and workmanship shall conform to IPC-A-600, Class 3 current revisions.
2) Board material and construction to be UL approved and marked on the finished board.
3) Laminate material: Copper-clad FR-4
4) Copper weight: 1 oz. finished
5) Finished thickness: 0.062” ±0.10”
6) MIN. plating thickness in through holes: 0.001”
7) SMOBC/HASL
8) LPI soldermask both sides using appropriate layer artwork: color = red
9) LPI silkscreen as required: color = white
10) Vendor information to be incorporated on back side whenever possible
11) Minimum copper conductor width is: 20 mils
    Minimum conductor spacing is: 10 mils
12) Number of finished layers: 4
13) Top and bottom layers 42-mil traces to be 50-Ω impedance

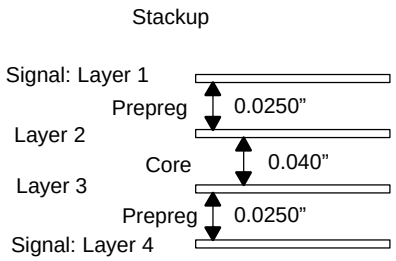


Figure 3-2. PWB Layer 1 (Signals)

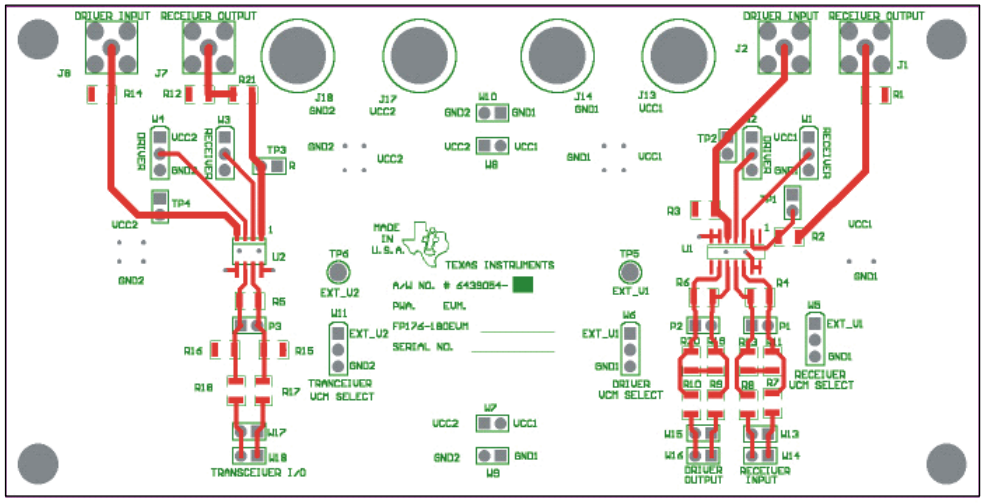


Figure 3-3. PWB Layer 2 (Split Ground Planes)

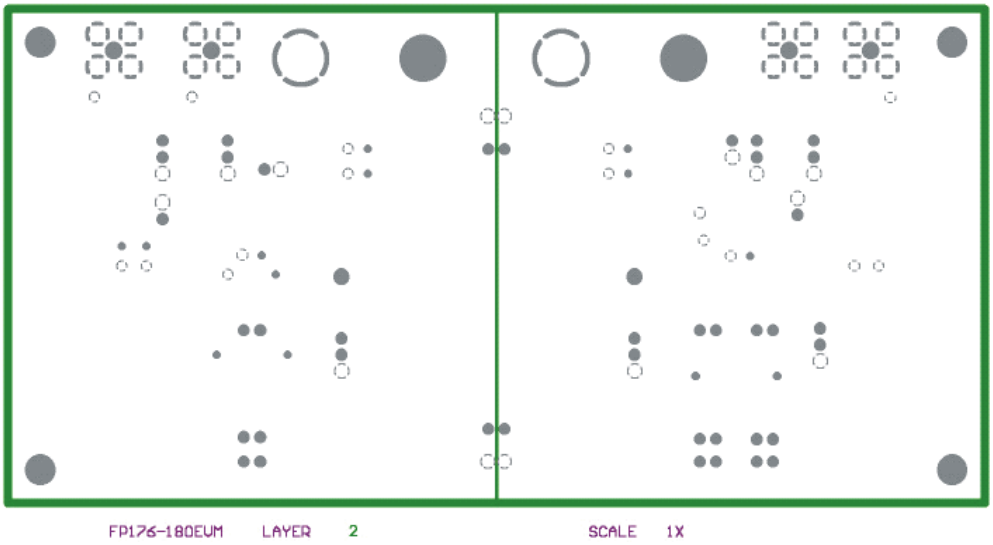


Figure 3-4. PWB Layer 3 (Split Power Planes)

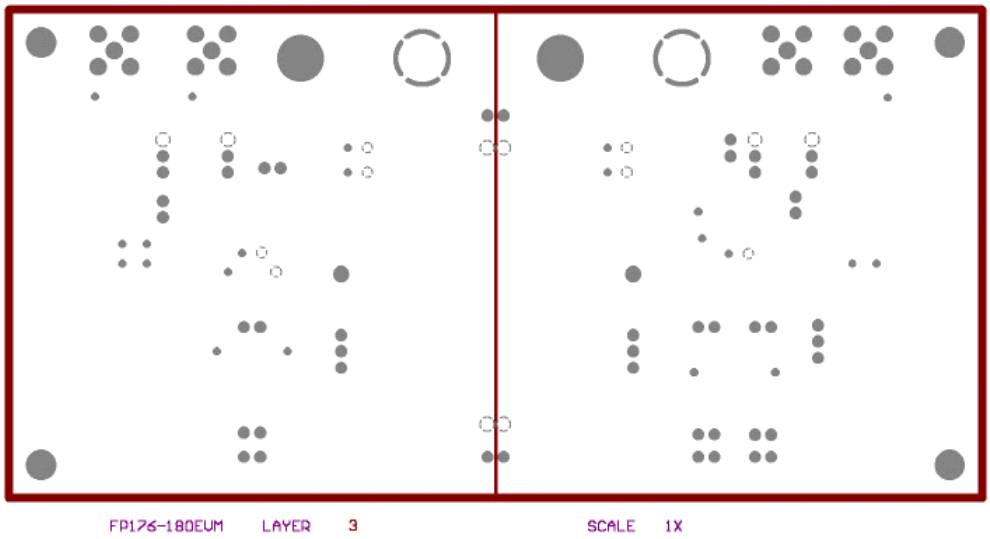
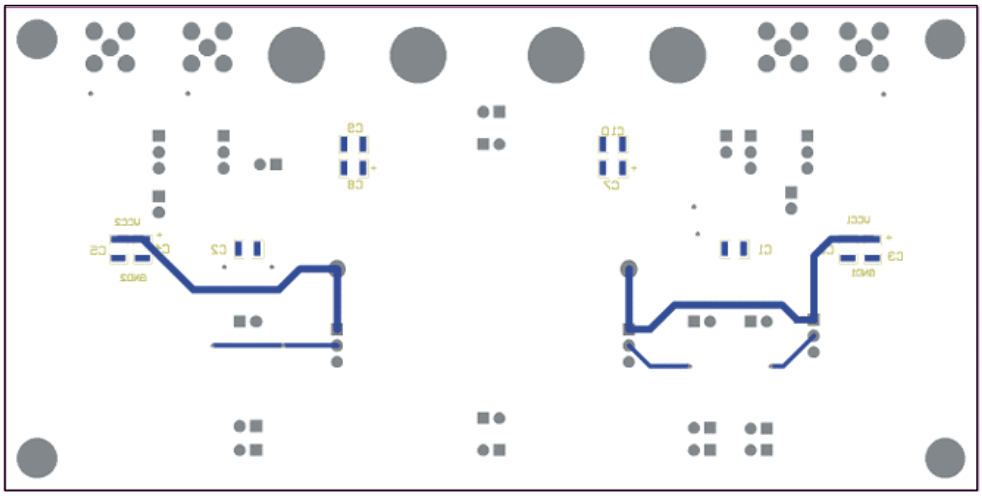


Figure 3-5. PWB Layer 4 (Signals)



3.2 Bill of Materials

	6439054								
Item No.	**-1 Qty**	**-2 Qty**	**-3 Qty**	**Part Description**	**MFR**	**Part Number**	**Package Style**	**Ref Des**	**Notes**
1	1			Board, printed wiring (PWB)	TI (K&S)	EIS No. 6439054			Blank PWB
2	1			Capacitor, 0.1 µF, ±10%, 16 V	Panasonic	ECJ-3VBIC104K	1206	C2	
3	2			Capacitor, 1.0 µF, ±10%, 16 V	Panasonic	ECJ-3VFIC105K	1206	C5, C9	
4	2			Capacitor, 10 µF, ±20%, 10 V Tant.	Panasonic	ECS-T1AY106R	”A”	C4, C8	
5	4			Jumper post, male, 2-Position	Amp	4-103239-0x2	100m ctrs	TP3, TP4, P3, W17	
6	1			Jumper post, female, 2-Position	Samtec	SS-102-G-1C	100m ctrs	W18	
7	3			Jumper post, male, 3-position	Amp	4-103239-0x3	100m ctrs	W3, W4, W11	Make From Item 5, Amp 4-103239-0
8	2			Resistor, 0.0 Ω, ±1%, 1/8 W	Dale	CRCW1206000F	1206	R17, R18	
9	1			Resistor, 100 Ω, ±1%, 1/8W	Dale	CRCW1206101F	1206	R5	
10	1			Resistor, 453 Ω, ±1%, 1/8W	Dale	CRCW1206453F	1206	R21	
11	3			Resistor, 51.1 Ω, ±1%, 1/8W	Dale	CRCW120651R1F	1206	R14, R15, R16	
12	1			Banana jack, black	Alectron	ST-351B		J18	
13	1			Banana jack, red	Alectron	ST-351A		J17	
14	2			SMA RF/ Coax. Conn., SMA Jack	Amphenol	901-144-8RFX		J7, J8	
15	3			Jumper short, Mini	BERG	65474-010	100m ctrs	W3,4,11	Install one each, from center to VCC
16	1			Test point, (yellow)	Keystone	5004K-ND		TP6	
17	4			Rubber mounting feet, (white)	BumpOn	SJ-5027			Install Last
18	1			Transceiver IC	TI	SN65HVD22	8-SOIC(D)	U2	

3.3 Schematic

The SN65HVD22EVM schematic, (17 in. X 11 in.) is furnished as an attachment to this chapter. Note that the EVM is populated with components for the SN65HVD22 transceiver (U2) only. The U1 circuit is not populated on the PWB.

Revision History		
REV	ECN Number	Approved
A	2026934, 02-26-2002	E. COLE

RECEIVER OUTPUT U1
J1
SMA
R2
453
(UNINSTALLED)
R1
51
TP1
VCC1
RECEIVER ENABLE
HI
LO
W1
W2
DRIVER ENABLE
C1
0.1uF
U1
NC
R
RE
DE
D
GND
GND
Vcc
Vcc
A
B
Z
Y
NC
FP_180
VCM SELECT
EXT_V1
W5
R7
0.0
R11
51
R13
51
R8
0.0
W13
W14
RECEIVER INPUT
R4
100
P1
DRIVER INPUT U1
J2
SMA
R3
51
TP2
EXT_V1
W6
R9
0.0
R19
51
R20
51
R10
0.0
W15
W16
DRIVER OUTPUT
R6
100
P2
RECEIVER OUTPUT U2
J7
SMA
R21
453
(UNINSTALLED)
R12
51
TP3
VCC2
RECEIVER ENABLE
W3
W4
DRIVER ENABLE
C2
0.1uF
U2
R
RE
DE
D
Vcc
B
A
GND
FP_176
VCM SELECT
EXT_V2
W11
R17
0.0
R15
51
R16
51
R18
0.0
W17
W18
TRANSCEIVER I/O
R5
100
P3
DRIVER INPUT U2
J8
SMA
R14
51
TP4
VCC1
J13
RED
J14
BLACK
C7
10uF
C10
1.0uF
VCC2
J17
RED
J18
BLACK
C8
10uF
C9
1.0uF
EXT_V1
TP5
C3
10uF
C6
1.0uF
EXT_V2
TP6
C4
10uF
C5
1.0uF
OPTIONAL
VCC1
W7
W8
VCC2
W9
W10

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: EVM SCHEMATIC, FP 176 / 180 6424409			
Engineer: E. COLE			
Drawn By:	SIZE: B	DATE: 27-Feb-2002	REV: A
FILE: Sheet1.Sch			SHEET: 1 OF: 1